NI SC Express

NI PXIe-4322 User Manual

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Contents

Chapter 1
Getting Started

Installation 1-1
Module Specifications 1-1
Module Accessories and Cables 1-1

Chapter 2
Using the NI PXIe-4322

Connecting Signals 2-1
    Increasing Output Voltage Range in Voltage Output Mode 2-2
    Increasing Output Current Range in Current Output Mode 2-3
Device Pinout 2-4
    I/O Connector Signal Description 2-6
NI PXIe-4322 Block Diagram 2-7
Analog Output Data Generation Methods 2-7
    Software-Timed Generations 2-7
    Hardware-Timed Generations 2-8
Analog Output Timing Signals 2-9
    AO Sample Clock Signal 2-9
        Using an Internal Source 2-9
        Using an External Source 2-10
        Routing AO Sample Clock Signal to an Output Terminal 2-10
        Other Timing Requirements 2-10
    AO Sample Clock Timebase Signal 2-10
Getting Started with AO Applications in Software 2-11
    External Reference Clock 2-11
        10 MHz Reference Clock 2-12
    Synchronizing Multiple Devices 2-13
    Triggering 2-13
        Digital Input Triggering 2-13
        TB-4322 Accessory 2-14
        Accessory Auto-Detection 2-14
        Isolation 2-14

Chapter 3
NI SC Express Considerations

PXI and NI SC Express Clock and Trigger Signals 3-1
    PXIe_CLK100 3-1
    PXIe_SYNC100 3-1
    PXI_CLK10 3-1
    PXI Triggers 3-1
    PXI_STAR Trigger 3-2

PXI_STAR Filters....3-2
PXIe_DSTAR <A..C>....3-2
Data Transfer Methods....3-3

Appendix A
Technical Support and Professional Services

List of Figures

Figure 2-1. Connecting a Load to a Channel Diagram....2-1
Figure 2-2. Output Circuit Grounding....2-1
Figure 2-3. Output Circuitry of One Channel Diagram....2-2
Figure 2-4. Cascaded Voltage Output Channels Diagram....2-3
Figure 2-5. Cascade Current Output Channels Diagram....2-4
Figure 2-6. NI PXIe-4322 Block Diagram....2-7
Figure 2-7. Analog Output Timing Options....2-9
Figure 2-8. AO Sample Clock and AO Start Trigger....2-10
Figure 2-9. External Clock Reference....2-12

List of Tables

Table 2-1. Front Signal Pin Assignments....2-5
Table 2-2. I/O Connector Signal Descriptions....2-6
Table 2-3. Clock Signal Sourcing....2-12

Table 3-1. PXIe_DSTAR Line Descriptions....3-2

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This product was tested and complies with the regulatory requirements and limits for electromagnetic compatibility (EMC) stated in the product specifications. These requirements and limits provide reasonable protection against harmful interference when the product is operated in the intended operational electromagnetic environment.

This product is intended for use in industrial locations. However, harmful interference may occur in some installations, when the product is connected to a peripheral device or test object, or if the product is used in residential or commercial areas. To minimize interference with radio and television reception and prevent unacceptable performance degradation, install and use this product in strict accordance with the instructions in the product documentation.

Furthermore, any modifications to the product not expressly approved by National Instruments could void your authority to operate it under your local regulatory rules.

Caution To ensure the specified EMC performance, operate this product only with shielded, twisted-pair cables and shielded accessories.

Caution To ensure the specified EMC performance, the length of all I/O cables must be no longer than 30 m (100 ft).

1 Getting Started

The NI PXIe-4322 provides eight, simultaneously updated, analog output channels, each with channel-to-channel and channel-to-earth isolation. Each channel has a 16-bit digital-to-analog converter (DAC) and can be configured as voltage output mode or current output mode. The voltage mode has ±16 V output range and the current mode has ±20 mA output range.

Installation

Refer to the *NI PXIe-4322 and TB-4322 Installation Guide and Terminal Block Specifications* for step-by-step software and hardware installation instructions.

Module Specifications

Refer to the *NI PXIe-4322 Specifications* document for module specifications.

Module Accessories and Cables

Refer to the *NI PXIe-4322 and TB-4322 Installation Guide and Terminal Block Specifications* document for information about supported accessories and cables.

Caution When hazardous voltages (>30 V_{rms}/42.4 V_{pk}/60 VDC) are present on any terminal, safety low-voltage (≤30 V_{rms}/42.4 V_{pk} /60 VDC) cannot be connected to any other terminal.

Caution Do *not* supply hazardous voltages (>30 V_{rms}/42.4 V_{pk}/60 VDC) to the terminal block without the terminal block being connected to the NI PXIe-4322.

2

Using the NI PXIe-4322

This chapter describes how to make connections to the NI PXIe-4322 module. It also provides the front signal pin assignments of the module.

Connecting Signals

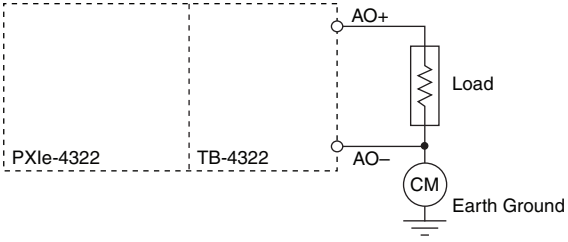
Note Refer to the *NI PXIe-4322 and TB-4322 Installation Guide and Terminal Block Specifications* document for details about signal terminal locations.

You can connect a load to each channel of the NI PXIe-4322. Connect the positive lead of the load to the AO+ terminal. Connect the ground of the load to the corresponding AO- terminal as shown in Figure 2-1.

Figure 2-1. Connecting a Load to a Channel Diagram

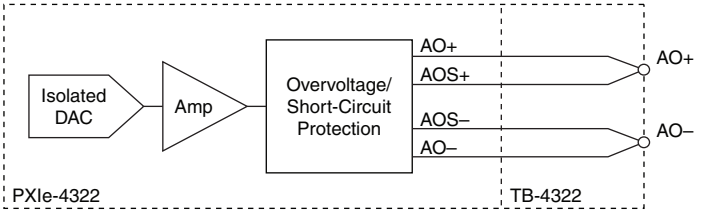
The analog output channels are floating with respect to earth ground and each other. If you make a ground-referenced connection between the signal source and the NI PXIe-4322 output, make sure the voltage on the AO+ and AO- connections are in the safety voltage range to ensure the proper operation. Refer to the *NI PXIe-4322 Specifications* for more information about Safety Voltage.

Figure 2-2. Output Circuit Grounding



Each channel has a DAC that produces a voltage or current signal. Each channel provides an independent signal path, enabling you to update all eight channels simultaneously. Each channel also has overvoltage and short-circuit protection. Refer to the *NI PXIe-4322 Specifications* for more information about the overvoltage and short-circuit protection. The output circuitry for one channel of the NI PXIe-4322 is shown in Figure 2-3.

Figure 2-3. Output Circuitry of One Channel Diagram



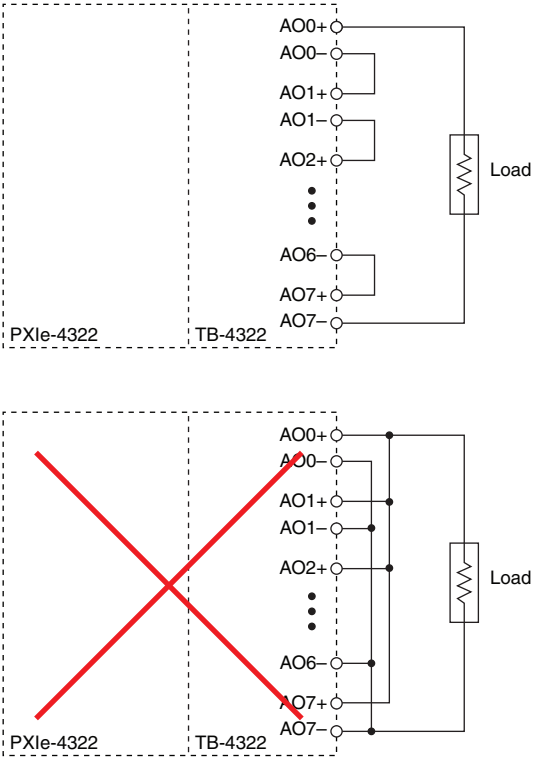
Increasing Output Voltage Range in Voltage Output Mode

Each channel of the NI PXIe-4322 has a nominal output voltage range of ±16 V and can drive up to ±20 mA of current. If you want to increase the nominal output voltage range, you can cascade up to eight output channels, as shown in Figure 2-4, for a maximum of ±128 V nominal.

Caution Cascading more than eight output channels of multiple NI PXIe-4322 modules violates overvoltage protection ratings.

Note The NI PXIe-4322 outputs can source and sink current; therefore, it is not possible to increase the current drive by connecting voltage output channels in parallel, as shown in the lower portion of Figure 2-4 and is indicated by being crossed out.

Figure 2-4. Cascaded Voltage Output Channels Diagram

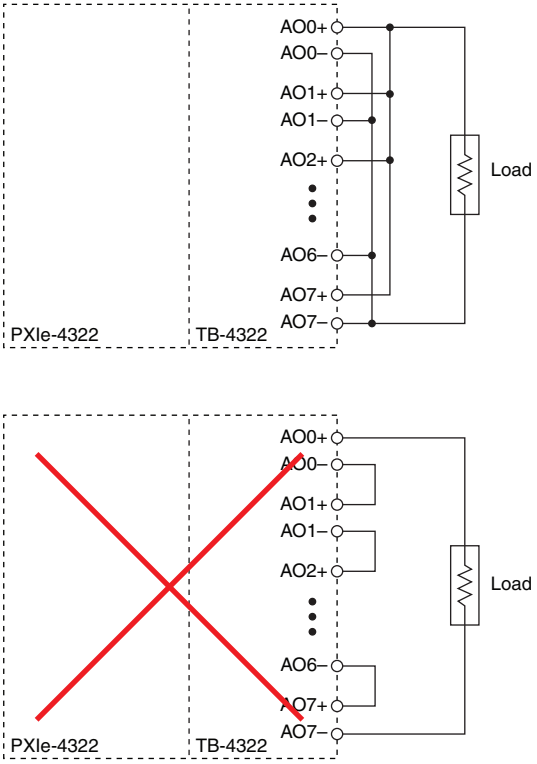


Increasing Output Current Range in Current Output Mode

Each channel of the NI PXIe-4322 has a nominal output current range of ±20 mA within its nominal compliance voltage of ±16 V. If you want to increase the nominal output current range, you can connect up to eight current mode output channels in parallel, as shown in Figure 2-5, for a maximum of ±160 mA nominal.

Note The NI PXIe-4322 output channels cannot be connected in series when they are in current mode, as shown in the lower portion of Figure 2-5 and is indicated by being crossed out.

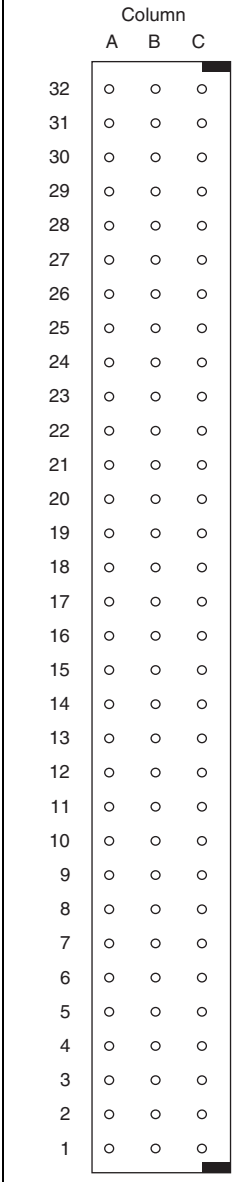
Figure 2-5. Cascade Current Output Channels Diagram



Device Pinout

This is the pinout represented on the front connector of the NI PXIe-4322. Refer to the *I/O Connector Signal Description* section for definitions of each signal. Refer to the terminal block installation guide for signal locations on the terminal block.

Table 2-1. Front Signal Pin Assignments

Front Connector Diagram	Pin Number	Column A	Column B	Column C	Channel
	32	—	AO 0+	AOS 0+	0
	31	—	AO 0-	AOS 0-	
	30	—	—	—	
	29	—	AO 1+	AOS 1+	1
	28	—	AO 1-	AOS 1-	
	27	—	—	—	
	26	—	AO 2+	AOS 2+	2
	25	—	AO 2-	AOS 2-	
	24	—	—	—	
	23	—	AO 3+	AOS 3+	3
	22	—	AO 3-	AOS 3-	
	21	—	—	—	
	20	—	AO 4+	AOS 4+	4
	19	—	AO 4-	AOS 4-	
	18	—	—	—	
	17	—	AO 5+	AOS 5+	5
	16	—	AO 5-	AOS 5-	
	15	—	—	—	
	14	—	AO 6+	AOS 6+	6
	13	—	AO 6-	AOS 6-	
	12	—	—	—	
	11	—	AO 7+	AOS 7+	7
	10	—	AO 7-	AOS 7-	
	9	—	—	—	
	8	—	—	—	No Channel
	7	—	—	—	
	6	—	—	—	
	5	—	—	—	
	4	—	—	—	
	3	—	—	—	
	2	RSVD	RSVD	RSVD	
	1	RSVD	RSVD	RSVD	
	— is no connection, RSVD is reserved				

I/O Connector Signal Description

Table 2-2 describes the signals found on the I/O connectors.

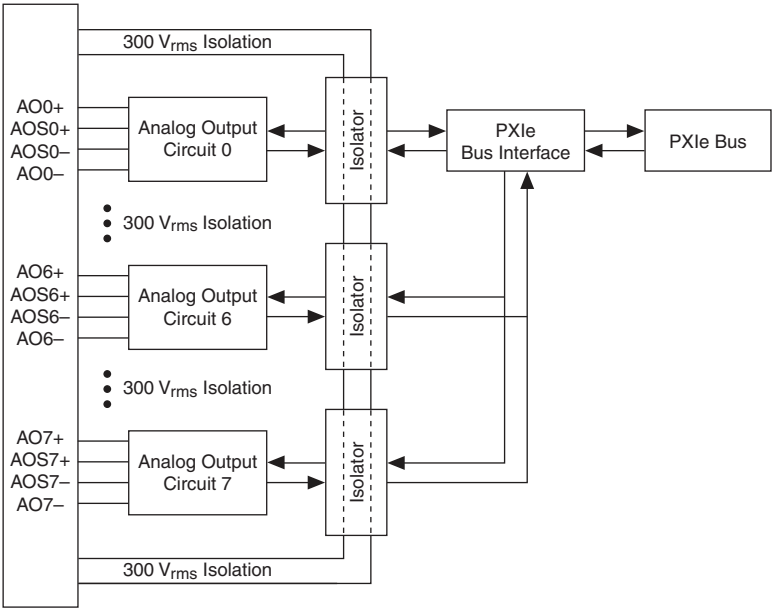
Table 2-2. I/O Connector Signal Descriptions

Signal Names	NI-DAQmx Signal Name	Description
AO <0..7>+, AO <0..7>-	AO <0..7>	Analog Output Channels 0 to 7. AO+ is the positive output terminal and AO- is the negative output terminal.
AOS <0..7>+, AOS <0..7>-	—	The sense lines of analog output channel 0 to 7. AOS+ is the positive sense line and AOS- is the negative sense line.
RSVD	—	These pins are reserved for communication with the accessory.
Notes: AOS± is connected to AO± at the terminal block user connector. When using a custom terminal block, connect AOS± to AO± at the terminal block.		

NI PXIe-4322 Block Diagram

Figure 2-6 shows the block diagram of the NI PXIe-4322 module.

Figure 2-6. NI PXIe-4322 Block Diagram



Analog Output Data Generation Methods

When performing an analog output operation, you can perform software-timed or hardware-timed generations.

Software-Timed Generations

With a software-timed generation, software controls the rate at which data is generated. Software sends a separate command to the hardware to initiate each DAC conversion. In NI-DAQmx, software-timed generations are referred to as on-demand timing. Software-timed generations are also referred to as immediate or static operations. They are typically used for writing a single value out, such as a constant DC voltage.

Hardware-Timed Generations

With a hardware-timed generation, a digital hardware signal controls the rate of the generation. This signal can be generated internally on your device or provided externally.

Hardware-timed generations have several advantages over software-timed generations:

- The time between samples can be much shorter.
- The timing between samples can be deterministic.
- Hardware-timed acquisitions can use hardware triggering.

Hardware-timed operations can be buffered or hardware-timed single point (HWTSP). A buffer is a temporary storage in computer memory for to-be-transferred samples.

- **Hardware-timed single point (HWTSP)**—Typically, HWTSP operations are used to write single samples at known time intervals. While buffered operations are optimized for high throughput, HWTSP operations are optimized for low latency and low jitter. In addition, HWTSP can notify software if it falls behind hardware. These features make HWTSP ideal for real-time control applications. HWTSP operations, in conjunction with the wait for next sample clock function, provide tight synchronization between the software layer and the hardware layer. Refer to the NI Developer Zone document, *NI-DAQmx Hardware-Timed Single Point Lateness Checking*, for more information. To access this document, go to `ni.com/info` and enter the Info Code `daqhwtsp`.
- **Buffered**—In a buffered generation, data is moved from a PC buffer to the onboard FIFO of the DAQ device using DMA before it is written to the DACs one sample at a time. Buffered generation typically allows for much faster transfer rates than non-buffered acquisitions because data is moved in large blocks, rather than one point at a time.

  One property of buffered I/O operations is the sample mode. The sample mode can be either finite or continuous:

  – Finite sample mode generation refers to the generation of a specific, predetermined number of data samples. Once the specified number of samples has been written out, the generation stops.

  – Continuous generation refers to the generation of an unspecified number of samples. Instead of generating a set number of data samples and stopping, a continuous generation continues until you stop the operation. There are several different methods of continuous generation that control what data is written. These methods are regeneration, FIFO regeneration and non-regeneration modes:

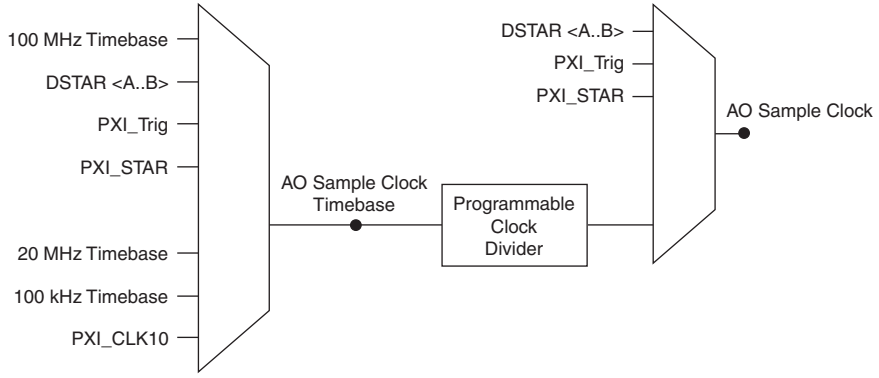
    - Regeneration is the repetition of the data that is already in the buffer. Standard regeneration is when data from the PC buffer is continually downloaded to the FIFO to be written out. New data can be written to the PC buffer at any time without disrupting the output. Use the NI-DAQmx write property RegenMode to allow (or not allow) regeneration. The NI-DAQmx default is to allow regeneration.

- With FIFO regeneration, the entire buffer is downloaded to the FIFO and regenerated from there. Once the data is downloaded, new data cannot be written to the FIFO. To use FIFO regeneration, the entire buffer must fit within the FIFO size. The advantage of using FIFO regeneration is that it does not require communication with the main host memory once the operation is started, thereby preventing any problems that may occur due to excessive bus traffic. Use the NI-DAQmx AO channel property, UseOnlyOnBoardMemory to enable or disable FIFO regeneration.
- With non-regeneration, old data is not repeated. New data must be continually written to the buffer. If the program does not write new data to the buffer at a fast enough rate to keep up with the generation, the buffer underflows and causes an error.

Analog Output Timing Signals

Figure 2-7 summarizes all of the timing options provided by the analog output timing engine.

Figure 2-7. Analog Output Timing Options



The NI PXIe-4322 features the following analog output (waveform generation) timing signals:

- *AO Sample Clock Signal* (digital filtering supported)
- *AO Sample Clock Timebase Signal* (digital filtering not supported)

AO Sample Clock Signal

Use the AO Sample Clock (ao/SampleClock) signal to initiate AO samples. Each sample updates the outputs of all of the DACs. You can specify an internal or external source for AO Sample Clock. You also can specify whether the DAC update begins on the rising edge or falling edge of AO Sample Clock.

Using an Internal Source

The AO Sample Clock Timebase (divided down) internal signal can drive AO Sample Clock.

A programmable internal counter divides down the AO Sample Clock Timebase signal.

Several other internal signals can be routed to AO Sample Clock through internal routes. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW Help* for more information.

Using an External Source

Use one of the following external signals as the source of AO Sample Clock:

- PXI_Trig <0..7>
- PXI_STAR
- PXIe-DSTAR<A,B>

Routing AO Sample Clock Signal to an Output Terminal

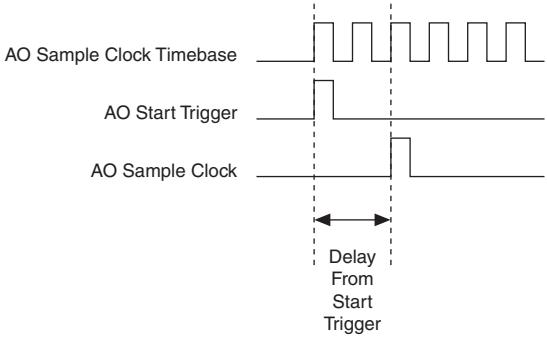
You can route AO Sample Clock (as an active low signal) out to any PXI_Trig <0..7>, or PXIe-DSTARC terminal.

Other Timing Requirements

The AO timing engine on your device internally generates AO Sample Clock unless you select some external source. AO Start Trigger starts the timing engine and either the software or hardware can stop it once a finite generation completes. When using the AO timing engine, you also can specify a configurable delay from AO Start Trigger to the first AO Sample Clock pulse. By default, this delay is two ticks of AO Sample Clock Timebase.

Figure 2-8 shows the relationship of AO Sample Clock to AO Start Trigger.

Figure 2-8. AO Sample Clock and AO Start Trigger



AO Sample Clock Timebase Signal

The AO Sample Clock Timebase (ao/SampleClockTimebase) signal is divided down to provide a source for AO Sample Clock.

You can route any of the following signals to be the AO Sample Clock Timebase signal:

- 100 MHz Timebase (default)

- 20 MHz Timebase
- 100 kHz Timebase
- PXI_CLK10
- PXI_Trig <0..7>
- PXI_STAR
- PXIe-DSTAR<A,B>

AO Sample Clock Timebase is not available as an output on the I/O connector.

You might use AO Sample Clock Timebase if you want to use an external sample clock signal, but need to divide the signal down. If you want to use an external sample clock signal, but do not need to divide the signal, then you should use AO Sample Clock rather than AO Sample Clock Timebase.

Getting Started with AO Applications in Software

You can use the NI PXIe-4322 modules in the following analog output applications:

- Single-point (on-demand) generation
- Finite generation
- Continuous generation
- Waveform generation

You can perform these generations through programmed I/O or DMA data transfer mechanisms. Some of the applications also use start triggers and pause triggers.

Note For more information about programming analog output applications and triggers in software, refer to the *NI-DAQmx Help* in NI-DAQmx 9.7 or later, or the *LabVIEW Help* in LabVIEW 2009 or later.

NI PXIe-4322 modules use the NI-DAQmx driver. NI-DAQmx includes a collection of programming examples to help you get started developing an application. You can modify example code and save it in an application. You can use examples to develop a new application or add example code to an existing application.

To locate LabVIEW, LabWindows™/CVI™, Measurement Studio, Visual Basic, and ANSI C examples, refer to the KnowledgeBase document, *Where Can I Find NI-DAQmx Examples?*, by going to `ni.com/info` and entering the Info Code `daqmxexp`.

For additional examples, refer to `zone.ni.com`.

External Reference Clock

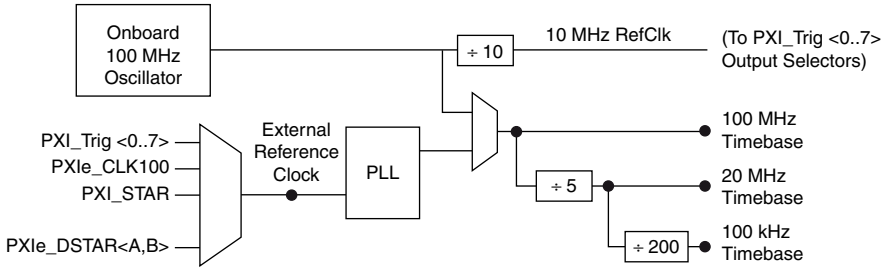
An external reference clock can be used as a source for the internal timebase on the NI PXIe-4322. This clock can be sourced using the signals shown in Table 2-3. Since the clock

is the input of a PLL, it must be 5 MHz, 10 MHz, 20 MHz, or 100 MHz. A PLL locks to the signal and produces a 100 MHz output, which is then divided down to produce the three timebases of 100 MHz, 20 MHz and 100 kHz. These timebases can then be used to generate sample clocks on the device. This circuit also enables the output of a 10 MHz RefClk that can be routed to PXI_Trig <0..7> and used by another device as its own External Reference Clock as shown in Figure 2-9.

Table 2-3. Clock Signal Sourcing

Signal	Description
PXI_Trig<0..7>	Bi-Directional bus connecting each board in the chassis.
PXIe_Clk100	100 MHz clock routed to all slots in the chassis.
PXI_STAR	Point-to-point route from the System Timing Slot to all other slots.
PXIe_DSTAR <A, B>	Point-to-point differential routes from the System Timing Slot to all other slots.

Figure 2-9. External Clock Reference



Caution Do not disconnect an external reference clock once the modules have been synchronized or are used by a task. Doing so may cause NI-DAQmx to return an error. Make sure that all tasks using a reference clock are stopped before disconnecting it.

10 MHz Reference Clock

The 10 MHz reference clock can be used to synchronize other devices to the NI PXIe-4322 module. The 10 MHz reference clock can be routed to the PXI_Trig <0..7> terminals. Other devices connected to the PXI_Trig bus can use this signal as a clock input.

The 10 MHz reference clock is generated by dividing down the onboard oscillator.

Synchronizing Multiple Devices

On PXI Express systems, you can synchronize devices to PXIe_CLK100. In this application the PXI Express chassis acts as the initiator. Each PXI Express module uses PXIe_CLK100 as its reference clock. Adding channels from multiple modules to the same NI-DAQmx task will perform synchronization automatically.

Another option in PXI Express systems is to use PXI_STAR. The Star Trigger controller device acts as the initiator and drives PXI_STAR with a clock signal. Each target module uses PXI_STAR as its external reference clock.

Sharing a trigger between multiple devices using PXI trigger lines introduces skew in the trigger signal, due to the propagation delay of the signal. The NI PXIe-4322 can compensate for that skew by locking the trigger to a clock (PXIe_SYNC100) that is derived from the reference clock (PXIe_CLK100). When you lock triggers to a clock, the device responds to those triggers on a subsequent edge of that clock, rather than immediately. Therefore, skew correction results in increased latency.

When you add multiple NI PXIe-4322 modules to the same NI-DAQmx task, NI-DAQmx automatically enables trigger skew correction. To enable trigger skew correction for applications that use multiple NI-DAQmx tasks, specify which device is the master and which devices are the slaves using the SyncType DAQmx Trigger property.

Triggering

The following sections provide details about analog and digital triggering of the NI PXIe-4322 module.

Digital Input Triggering

You can configure the NI PXIe-4322 device to start or pause an acquisition in response to a digital trigger signal from either PXIe_DSTAR <A, B>, PXI_Trig<0..7>, or PXI_STAR. The trigger circuit can respond to a rising, falling, or level sensitive signal, in one of the following three modes:

- **Start**—Begins an acquisition when trigger is met.
- **Reference**—A certain number of pre-trigger and post-trigger samples are specified around the trigger.
- **Pause**—Acquisition is put on hold when trigger is met (level sensitive only).

In addition, the trigger circuit provides a programmable filter to help with noisy trigger signals. The filter checks that the trigger condition is met for different time intervals before triggering. The filter can select from 90 ns, 5.12 µs, 2.56 ms, or a custom defined time interval. For information about configuring digital filters, refer to the *NI-DAQmx Help*.

TB-4322 Accessory

The TB-4322 terminal block provides screw terminals for access to the module. The TB-4322 is strictly a feedthrough terminal block.

Accessory Auto-Detection

NI SC Express modules automatically detect compatible accessories or terminal blocks. The RSVD pins on the I/O connector provide power to the accessories as well as digital communication lines. This allows software to detect when accessories are inserted or removed. In addition, software can automatically identify the specific terminal block as well as access any scaling information associated with the terminal block.

MAX allows you to see what accessories are currently connected to your module. In MAX, expand **Devices and Interfaces** and locate your module. If a terminal block is connected to your module, it will be displayed beneath the module. Unsupported terminal blocks appear in MAX with an X next to them.

NI-DAQmx property nodes can be used to programmatically access information about connected accessories in your application. Refer to the *NI-DAQmx Help* for documentation about programmatically accessing accessory status. Select **Start»All Programs»National Instruments»NI-DAQ»NI-DAQmx Help**.

Accessory Power

The NI PXIe-4322 provides auxiliary power for accessories connected to the module and has protection in the event of a fault condition. If a fault occurs in the form of an over-power condition, the power supply latches off until it is reset. To reset after a fault condition perform a Device Reset in MAX or programmatically in your ADE.

Isolation

Caution Refer to the *Read Me First: Safety and Electromagnetic Compatibility*, included with your module, for more safety information.

The NI PXIe-4322 provides 300 V channel-to-channel basic isolation as well as 300 V channel-to-earth reinforced isolation. This rating is intended for measurements within Measurement Category II. These isolation levels are verified with a five-second dielectric withstand test. Refer to the *NI PXIe-4322 Specifications* for details.

Measurement Category II is for measurements performed on circuits directly connected to the electrical distribution system. This category refers to local-level electrical distribution, such as that provided by a standard wall outlet, for example, 115 V for U.S. or 230 V for Europe.

Do not connect the NI PXIe-4322 module to signals or use for measurements within Measurement Categories III or IV.

3

NI SC Express Considerations

PXI clock and trigger signals are only available on PXI Express devices.

PXI and NI SC Express Clock and Trigger Signals

PXIe_CLK100

PXIe_CLK100 is a common low-skew 100 MHz reference clock for synchronization of multiple modules in a PXI Express measurement or control system. The PXIe backplane is responsible for generating PXIe_CLK100 independently to each peripheral slot in a PXI Express chassis. For more information, refer to the *PXI Express Specification* at `www.pxisa.org`.

PXIe_SYNC100

PXIe_SYNC100 is a common, low-skew 10 MHz reference clock with a 10% duty cycle for synchronization of multiple modules in a PXI Express measurement or control system. The PXI Express backplane is responsible for generating PXIe_SYNC100 independently to each peripheral slot in a PXI Express chassis. For more information, refer to the *PXI Express Specification* at `www.pxisa.org`.

PXI_CLK10

PXI_CLK10 is a common low-skew 10 MHz reference clock for synchronization of multiple modules in a PXI measurement or control system. The PXI backplane is responsible for generating PXI_CLK10 independently to each peripheral slot in a PXI chassis.

Note PXI_CLK10 cannot be used as a reference clock for SC Express modules.

PXI Triggers

A PXI chassis provides eight bused trigger lines to each module in a system. Triggers may be passed from one module to another, allowing precisely timed responses to asynchronous external events that are being monitored or controlled. Triggers can be used to synchronize the operation of several different PXI peripheral modules.

On SC Express modules, the eight PXI trigger signals are synonymous with PXI_Trig <0..7>.

Note that in a PXI chassis with more than eight slots, the PXI trigger lines may be divided into multiple independent buses. Refer to the documentation for your chassis for details.

PXI_STAR Trigger

In a PXI Express system, the Star Trigger bus implements a dedicated trigger line between the system timing slot and the other peripheral slots. The Star Trigger can be used to synchronize multiple devices or to share a common trigger signal among devices.

A Star Trigger controller can be installed in this system timing slot to provide trigger signals to other peripheral modules. Systems that do not require this functionality can install any standard peripheral module in this system timing slot.

An SC Express module receives the Star Trigger signal (PXI_STAR) from a Star Trigger controller. PXI_STAR can be used as an external source for many AI, AO, and counter signals.

An SC Express module is not a Star Trigger controller. An SC Express module can be used in the system timing slot of a PXI system, but the system will not be able to use the Star Trigger feature.

PXI_STAR Filters

You can enable a programmable debouncing filter on each PXI_Trig, PXIe_DSTAR, or PXI_STAR signal.

PXIe_DSTAR <A..C>

PXI Express devices can provide high-quality and high-frequency point-to-point connections between each slot and a system timing slot. These connections come in the form of three low-voltage differential star triggers that create point-to-point, high-frequency connections between a PXI Express system timing module and a peripheral device. Using multiple connections enable you to create more applications because of the increased routing capabilities.

Table 3-1 describes the three differential star (DSTAR) lines and how they are used.

Table 3-1. PXIe_DSTAR Line Descriptions

Trigger Line	Purpose
PXIe_DSTARA	Distributes high-speed, high-quality clock signals from the system timing slot to the peripherals (input).
PXIe_DSTARB	Distributes high-speed, high-quality trigger signals from the system timing slot to the peripherals (input).
PXIe_DSTARC	Sends high-speed, high-quality trigger or clock signals from the peripherals to the system timing slot (output).

The DSTAR lines are only available for PXI Express devices when used with a PXI Express system timing module. For more information, refer to the *PXI Express Specification* at `www.pxisa.org`.

Data Transfer Methods

The primary ways to transfer data across the PCI Express bus are as follows:

- **Direct Memory Access (DMA)**—DMA is a method to transfer data between the device and computer memory without the involvement of the CPU. This method makes DMA the fastest available data transfer method. NI uses DMA hardware and software technology to achieve high throughput rates and increase system utilization. DMA is the default method of data transfer for PCI Express and PXI Express devices.
- **Programmed I/O**—Programmed I/O is a data transfer mechanism where the user's program is responsible for transferring data. Each read or write call in the program initiates the transfer of data. Programmed I/O is typically used in software-timed (on-demand) operations.

A

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